

| Course Number | COE328 |
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| Course Title | Digital Systems - F2022 |
| Semester/Year | Fall 2022 |
| Instructor | Shazzat Hossain |
| TA Name | Sajjad |

| Lab/Tutorial Report No. | Lab 5 |
| --- | --- |

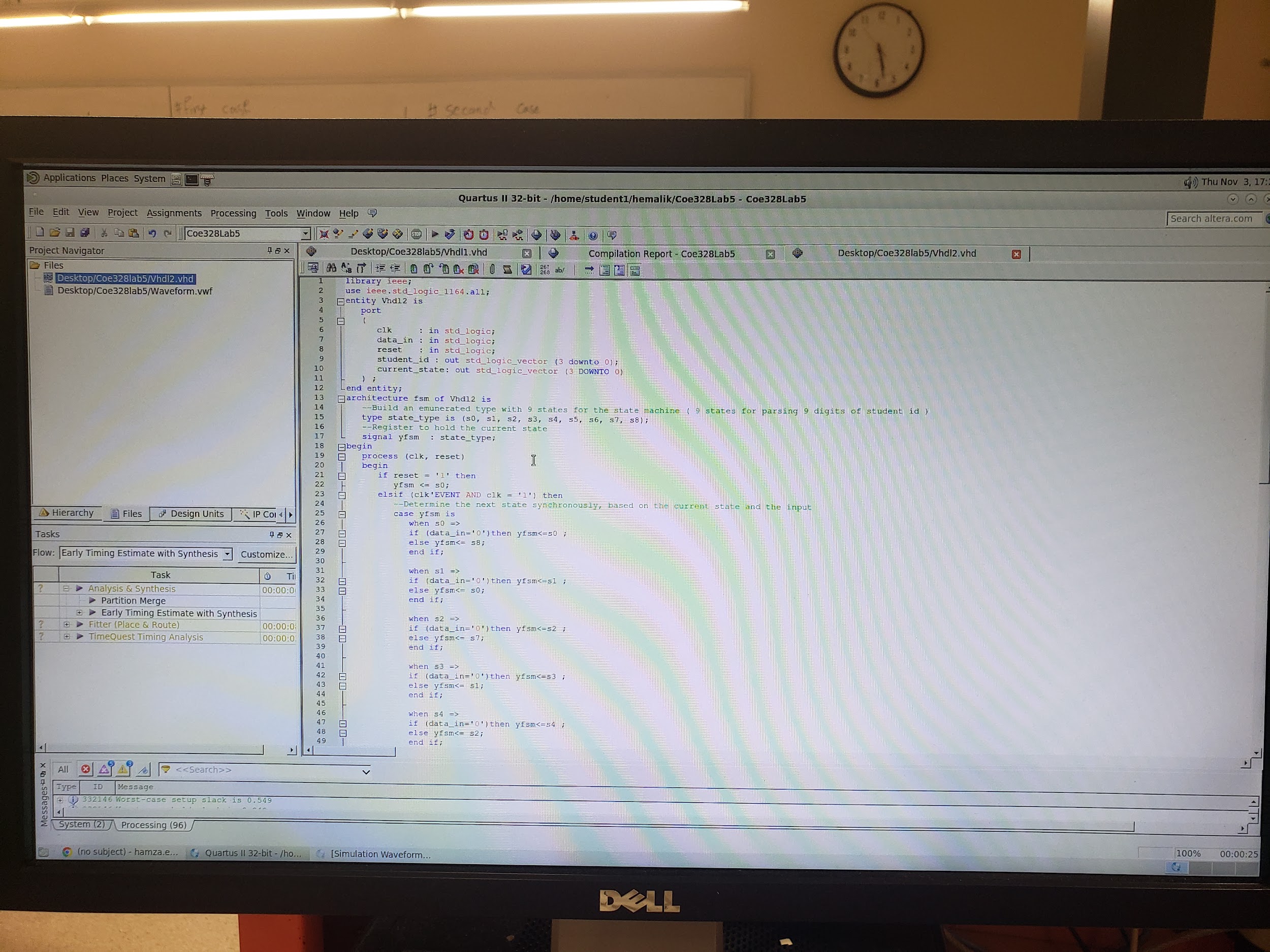
| Report Title | **VHDL for Sequential Circuits: Implementing a customized State Machine** |
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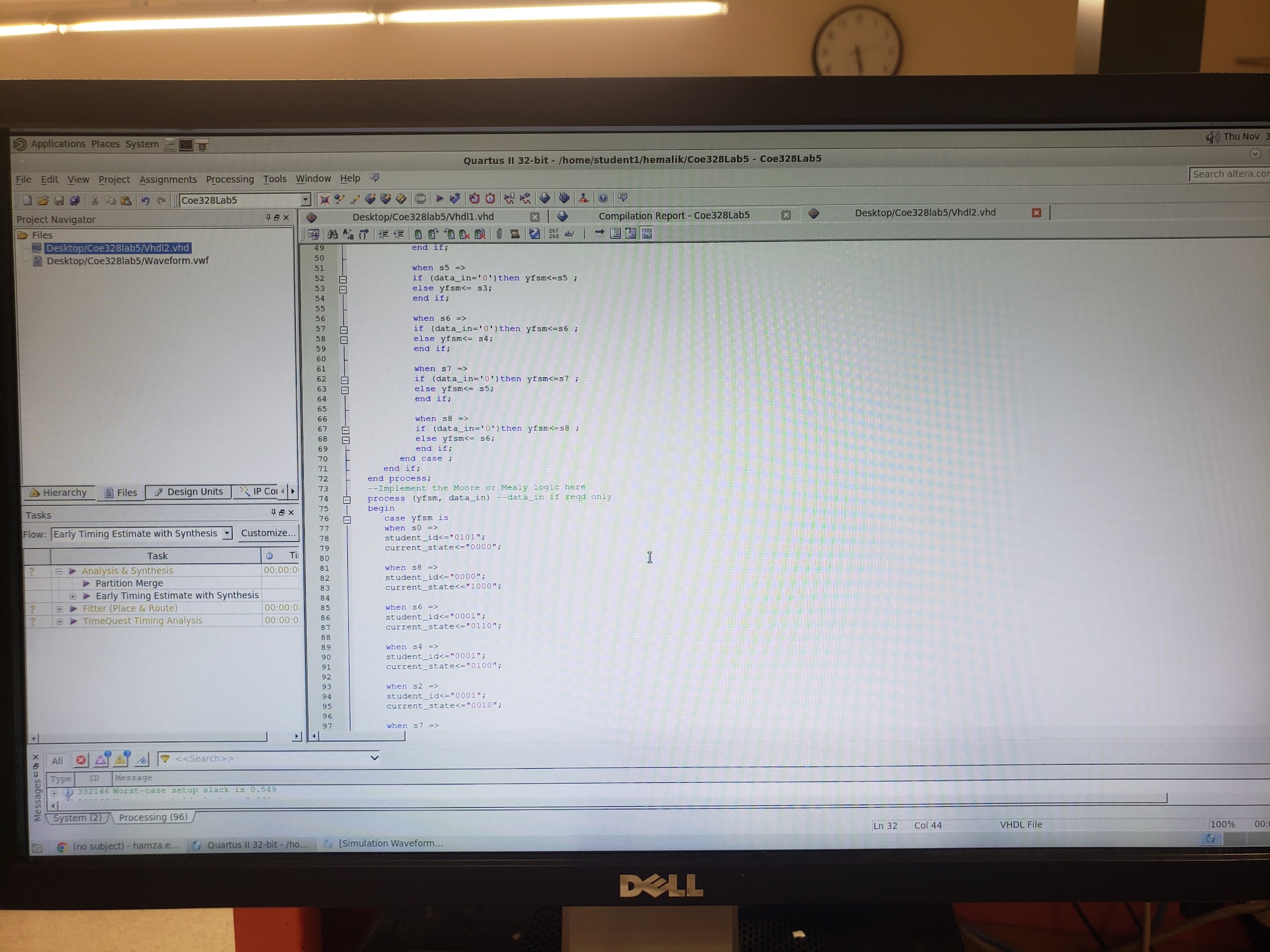
| Section No. | 11 |
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| Group No. | N/A |
| Submission Date | Nov 18, 2022 |
| Due Date | Nov 18, 2022 |

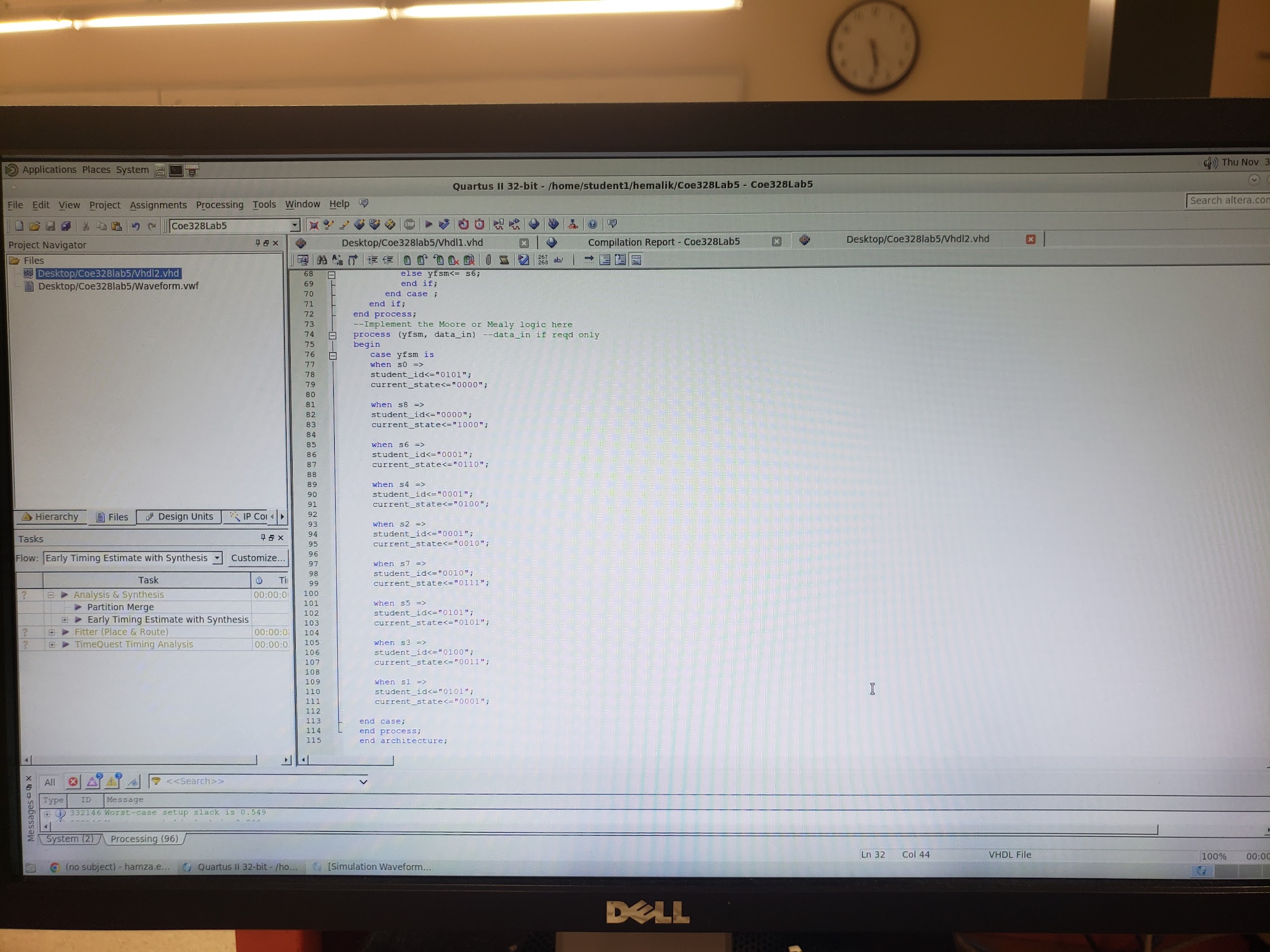
| Student Name | Student ID | Signature\* |
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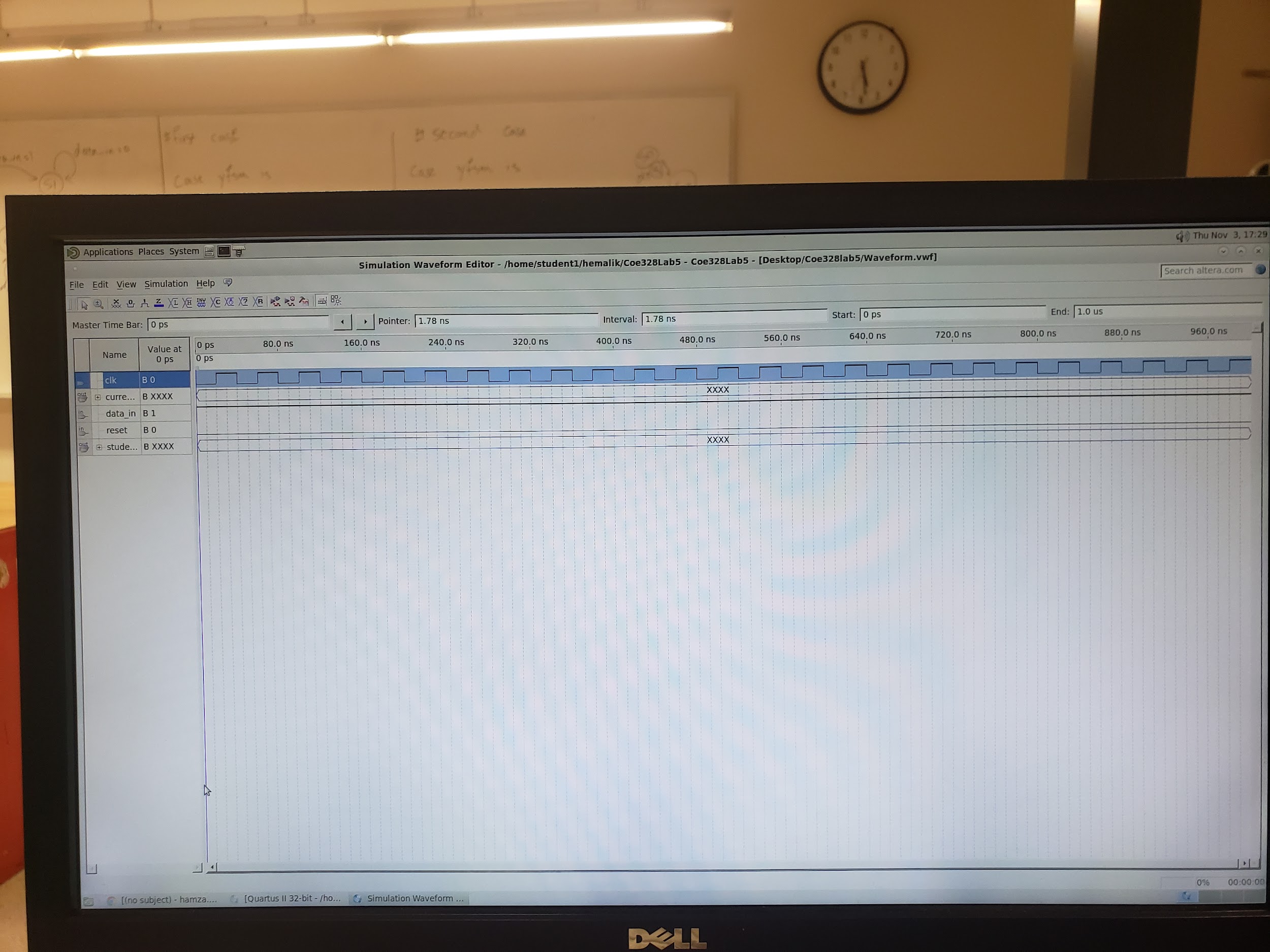
[*http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf*](http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf)







This is the VHDL Skeleton code for lab5 coe328 created during our lab 5 with the custom function.



This is a picture of our block diagram schematics created with the VHDL code.

**Conclusion:**

To wrap up our lab 5, we implemented a customized State Machine corresponding Mealy/Moore machine state diagrams for representing student ID in order to design a finite state machine (FSM) that cycles through the individual digits of our student ID using the assigned state diagrams. We wrote our vdhl code with the new custom function and compiled it and after that we got an output for the diagram schematic.